Clean version of all pending claims

1. (Amended once) A system comprising:

a processor; and

a memory device coupled to the processor and contained within a single integrated circuit, the memory device including:

a main memory; and

a cache memory coupled to the processor and to the main memory to store data from non-consecutive addresses requested from the main memory.

2. (Amended once) The system of claim 1, wherein:

all circuitry to operate the cache memory is contained within the memory device.

3. The system of claim 1, wherein:

the main memory is a flash memory.

4. The system of claim 1, wherein:

the cache memory can hold no more than sixteen addresses at the same time.

5. (Amended once) The system of claim 1, wherein:
the processor is contained within the single integrated circuit.

6. (Amended once) An apparatus comprising:
a memory device to couple to a processor through a bus, the memory device including on a single integrated circuit:
a main memory; and
a cache memory coupled to the main memory to store data from non-consecutive addresses requested from the main memory.

7. (Amended once) The apparatus of claim 6, wherein:
all circuitry to operate the cache memory is contained within the single integrated circuit.

8. The apparatus of claim 6, wherein:
the main memory is a flash memory.

9. The apparatus of claim 6, wherein:
the cache memory can hold no more than sixteen addresses at one time.

10-20. (Cancelled)